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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/046,937	01/14/2002	Jeff C. Klein	H0002065	4430

128 7590 10/20/2004

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EXAMINER
KERVEROS, JAMES C

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 10/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)	
	10/046,937	KLEIN ET AL.	
	Examiner	Art Unit	
	JAMES C KERVEROS	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-53* is/are pending in the application.

4a) Of the above claim(s) *25-53* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 May 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/23/02,9/8/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I (Claims 1-24) in the reply filed on 6/10/2004 is acknowledged.

Claims 25-53 withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 6/10/2004.

Claims 1-53 are pending and Claims 1-24 are hereby presented for examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-7, 13-18 and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Winter et al. (US 6021271), ISSUED: February 1, 2000.

Regarding independent Claims 1, 13 , 24 and dependent claims 2, 3, 7, 14, 18, Winter discloses a method of verifying proper design and operation of a programmed programmable logic device (PLD), such as an integrated circuit based on an electronic circuit design, comprising:

Developing a simulation test vector such as a simulation input file (step 100), flow diagram, Figure 2, using a PLD design automation software tool, such as a computer or data processor which has an assembler, compiler, for testing a simulated model of the programmed PLD such as an (integrated circuit 20, Figure 1) that includes an electrically programmable read-only memory (EPROM) cell within the memory 24.

Translating the simulation test vector (simulation input file, step 100) into a device level test vector (step 102), which processed the simulation input file to generate object code readable by the PLD test device.

Testing (step 106) the programmed PLD (integrated circuit 20, Figure 1) using each of the device level test vectors (object code) to obtain device (20) level test results. According to (step 106), a simulation program is run using the object code to simulate the electronic circuit design of integrated circuit 20 and to test the electronic circuit design. As part of the simulation, test vectors are generated that represent the status of the electrodes of the electronic circuit design for each instruction in the object code.

Testing the simulated model, which is generated of the electronic design of the integrated circuit 20 (step 104) and includes a hardware representation of that electronic circuit design, to obtain simulation test results (step 106).

Comparing the simulation test results with the device level test results in the simulation results file (step 108) to confirm the simulation was successful. If not, the simulation input file or the model file can be modified and the simulation run again.

Regarding independent Claim 24, in addition to the pertinent limitations recited in the independent claim 13, Winter discloses a method of verifying proper design and operation of a programmed programmable logic device (PLD), such as an integrated circuit based on an electronic circuit design, including the limitations of:

Developing a software model of the programmed PLD using a design automation software tool. According to (step 104), "a model file is generated of the electronic design of the integrated circuit 20. The model file includes a hardware representation of that electronic circuit design. The model file may be generated by a person or a machine including a computer, data processor, or the like".

Translating the software model (step 104) of the programmed PLD (20) into a simulated model of the programmed PLD using a simulation software tool. According to (step 106), "a simulation program is run using the object code, entry table, comment table, and model file to simulate the electronic circuit design of integrated circuit 20".

Regarding Claims 4-6, 15-17, Winter discloses developing a software model (step 104) of the integrated circuit 20, which includes a hardware representation of the electronic circuit design, using the design automation software tool, such as a machine including a computer or a data processor. Also, the simulation software performs translating the simulation test vector (simulation input file, step 100) into a device level test vector (step 102), which processed the simulation input file to generate object code readable by the PLD test device. The device level test vectors include stimulus data and expected results data. "The test vectors generated from the test input file are

used to drive inputs and verify outputs from the integrated circuit 20". The stimulus data correspond to (drive inputs) and expected results data correspond to (verify outputs).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 8 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Winter et al. (US 6021271).

Regarding Claims 8, 19, Winter does not explicitly disclose compressing and decompressing the compressed data files to recover the device level test vectors. However, it is well known in the art to compress and decompress data for storage purpose. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use well known compression and decompression data storage techniques, in the method of Winter, for the purpose of storing and retrieving test vectors from a storage device. A person skilled in the art would have been motivated to use compression and decompression techniques, so as to save memory space.

4. Claims 9-12 and 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Winter et al. (US 6021271) in view of Joly et al. (US 6178541).

Regarding Claims 9-12, 20-23, winter does not explicitly disclose synthesizing the software model of the programmed PLD using a design synthesis software tool. However, Joly et al. (US 6178541), in an analogous art, discloses a method including a behavioral model HDL, which is typically manipulated with an appropriate ADE synthesis tool to produce a register transfer level (RTL) description of subsystem 202a, Figure 3. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use an appropriate ADE synthesis tool, as taught by Joly, in the method of Winter. A person skilled in the art would have been motivated to employ a design synthesis software tool, so as to reduce the design cycle time for a complex ASIC by breaking the synthesis, layout, and verification tasks into modular units associated with the various subsystems of the target device.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Simunic et al. (US 5923567) discloses a method and device for test vector analysis, Figure 1, illustrating a block diagram form a prior art manufacturing process, including a device design 115 described by the net-list used together with simulation input 117 for the simulator to test the device design and provide simulation output 119. Vector processing software takes the simulation output and generates test vectors 125 which are to be input into a digital IC tester.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C KERVEROS whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

U.S. PATENT OFFICE
Examiner's Fax: (703) 746-4461
Email: james.kerveros@uspto.gov

Date: 14 October 2004
Office Action: Non-Final Rejection

By: _____

JAMES C KERVEROS
Examiner
Art Unit 2133

GAY J. LAMARRE
PRIMARY EXAMINER